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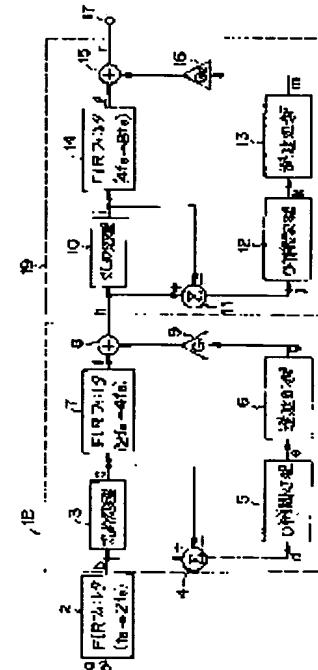
(21)Application number : 05-068351 (71)Applicant : SONY CORP
 (22)Date of filing : 26.03.1993 (72)Inventor : TOYODA TAKASHI

(54) DIGITAL SIGNAL ARITHMETIC UNIT

(57)Abstract:

PURPOSE: To reduce a rounding error i.e., a re-quantization error in an audible zone without increasing a hardware scale by taking out a generated rounding error by a rounding error extraction means, and eliminating a superimposed rounding error component from the output of a rounding processing means by a rounding error elimination means by using the rounding error.

CONSTITUTION: A digital filter means 7 with (m) bits of allowable input word length, the rounding processing means 3 which performs the rounding processing of input of (n) bits longer than the (m) bits of allowable input word length to (m) bits, and the rounding error extraction means 4 which takes out the rounding error from the output of the rounding processing means 3 are provided. The rounding error component superimposed on the filter output of the digital filter means 7 is eliminated by the rounding error elimination means 8 by using the rounding error taken out by the rounding error extraction means 4. This digital signal arithmetic unit can be constituted by setting it as one block 18 cascade connecting plural of the blocks, and forming them in multiple stage constitution.



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